

What is claimed is:

- 1           1. A method of transmitting data over a source synchronous communications  
2 interface, the method comprising:  
3           (a) receiving a source synchronous data strobe signal driven by a data  
4 source during a data transfer from the data source; and  
5           (b) disabling a data latch from latching data received from the data source  
6 whenever the data source is not driving the source synchronous data strobe signal.
- 1           2. The method of claim 1, wherein disabling the data latch comprises gating the  
2 source synchronous data strobe signal.
- 1           3. The method of claim 2, wherein gating the source synchronous data strobe  
2 signal comprises applying a gate signal to the data latch that enables latching by the data  
3 latch only when the gate signal is asserted, wherein the gate signal is asserted proximate a  
4 start of a data transfer from the data source, and deasserted proximate an end of the data  
5 transfer from the data source.
- 1           4. The method of claim 3, wherein applying the gate signal comprises asserting  
2 the gate signal responsive to a synchronous enable signal that is asserted proximate the  
3 start of the data transfer from the data source.
- 1           5. The method of claim 4, wherein applying the gate signal further comprises  
2 deasserting the gate signal responsive to a synchronous postamble signal that is asserted  
3 proximate the end of the data transfer from the data source.
- 1           6. The method of claim 1, further comprising locally tracking progress of the data  
2 transfer from the data source.

1           7. The method of claim 6, wherein locally tracking the progress of the data  
2 transfer includes counting cycles of the source synchronous data strobe signal to track  
3 data transfer cycles during a data transfer from the data source.

1           8. The method of claim 7, wherein locally tracking the progress of the data  
2 transfer further includes indicating whenever the number of data transfer cycles is  
3 equivalent to a burst length for the data transfer.

1           9. The method of claim 1, wherein the data source comprises a synchronous  
2 dynamic random access memory (SDRAM), and wherein the source synchronous  
3 communications interface comprises an SDRAM memory interface.

1           10. The method of claim 9, wherein the data source comprises a double data rate  
2 (DDR) SDRAM, and wherein the source synchronous communications interface  
3 comprises a DDR SDRAM memory interface.

1           11. The method of claim 1, wherein gating the source synchronous data strobe  
2 signal comprises:

3                   (a) incrementing a counter and outputting a burst length signal that  
4 indicates whether the counter stores a value equivalent to a predetermined burst  
5 length;

6                   (b) performing a logical AND operation on the burst length signal and a  
7 synchronous postamble signal and outputting therefrom a first output signal,  
8 wherein the synchronous postamble signal is asserted proximate the end of a data  
9 transfer from the data source;

10                  (c) performing a logical OR operation on the first output signal and a  
11 synchronous enable signal and outputting therefrom a gate signal, wherein the  
12 synchronous enable signal is asserted during the data transfer from the data  
13 source; and

1                   (d) performing a logical AND operation on the gate signal and the source  
2                   synchronous data strobe signal and outputting therefrom a gated source  
3                   synchronous data strobe signal that is coupled to the data latch.

1                   12. The method of claim 11, wherein incrementing the counter is performed in  
2                   response to a logically-inverted gated source synchronous data strobe signal, and wherein  
3                   the method further comprises logically-inverting the burst length signal prior to  
4                   performing the logical AND operation.

1                   13. The method of claim 1, wherein disabling the data latch comprises controlling  
2                   a select input on a multiplexer coupled to an input of the data latch to select a first input  
3                   among first and second inputs for the multiplexer, wherein the first input of the  
4                   multiplexer is coupled to an output of the data latch, and the second input of the  
5                   multiplexer is coupled to receive the data from the data source.

1                   14. The method of claim 1, wherein the source synchronous data strobe signal  
2                   comprises a DQS signal from a synchronous dynamic random access memory (SDRAM)  
3                   during a transfer of read data from the SDRAM.

- 1           15. A method of transferring read data from a synchronous dynamic random
- 2           access memory (SDRAM) over a source synchronous communications interface, the
- 3           method comprising:
- 4                 (a) receiving a source synchronous DQS signal driven by the SDRAM
- 5                 during a data transfer of read data from the SDRAM; and
- 6                 (b) selectively disabling a data latch from latching data received from the
- 7                 SDRAM source whenever the SDRAM is not driving the DQS signal.